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| EXAMINER | |
|---|---|
| PATEL, KAUSHIKKUMAR M | |
| ART UNIT | PAPER NUMBER |
| 2188 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/541,284 | NASE, RAINER | |
| | Examiner | Art Unit | |
| | KAUSHIKKUMAR PATEL | 2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-5,7,10 and 12-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,10 and 12-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. This Office Action is in response to applicant's communication filed March 18, 2008 in response to PTO Office Action mailed October 18, 2007. The applicant's remarks and amendments to the claims and/or specification were considered with the results that follow.

2. In response to last Office Action, claims 1, 10 and 12-14 have been amended. Claims 6, 8, 9 and 11 have been canceled. Claims 15-17 have been added. As a result, claims 1-5, 7, 10 and 12-17 remain pending in this application.

### *Response to Arguments*

3. Applicant's arguments filed March 18, 2008 have been fully considered but they are not fully persuasive.

Applicant argues that Sassa does not address the smart card controller memory problem because Sassa's focus is a flash memory which, within Applicant's knowledge, is installed in memory cards, digital cameras and the like and Sassa has no reference whatsoever to a persistent memory. The examiner respectfully disagrees with the fact because a flash memory indeed is a persistent memory because it does not loose data when power is turned off. Further, the limitation appears in preamble of the claim 1 and 15 and recites intended purpose for the method, e.g. "A method for memory management in smart card controllers" and according to MPEP § 2111.02:

"The claim preamble must be read in the context of the entire claim. The determination of whether preamble recitations are structural limitations or mere statements of purpose or use "can be resolved only on review of the entirety of the [record] to gain an understanding of what the inventors actually invented and intended to encompass by the claim." Corning Glass Works, 868 F.2d at 1257, 9 USPQ2d at 1966. If the body of a claim fully and intrinsically sets forth all of the limitations of the claimed invention, and the preamble merely states, for example, the purpose or intended use of the invention, rather than any distinct definition of any of the claimed invention's limitations, then the preamble is not considered a limitation and is of no significance to claim construction. Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1305, 51 USPQ2d 1161, 1165 (Fed. Cir. 1999). See also Rowe v. Dror, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997) ("where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention, the preamble is not a claim limitation")".

"A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951)".

Applicant argues that Sassa does not teach or suggest step b) of the claim (e.g. selecting the variable size of the block). However as admitted by the applicant, Sassa

teaches plurality of blocks and each block having fixed length (remarks, page 8), where it is readily apparent that the size of the logical block is equivalent to the size of the physical block, where physical block can include any number of pages (e.g. 1, 2, 16 etc.) of size 528 bytes and since the logical block is equal to size of the physical block, the limitation "selecting the size of the blocks as such that it is equal to or equivalent to an inter ratio of the length of the page in EEPROM" is satisfied by having logical block size equal to the size of the physical block, where physical block contains integer ratio of the physical pages (e.g. 528 bytes for each page) of the memory.

Applicant further argues that Sassa does not teach any reference at all to a linkage with the identified function (remarks, page 10). The examiner respectfully disagrees with the fact. As mentioned in previous office action, col. 6, line 39 - col. 7, line 5 does teach linkage with the other block by writing address of the block to be linked with ("The "logical address" indicates a logical address of the block. The "linkage address" indicates a logical address of a block to be linked with this block", col. 6, lines 61-63).

Applicant's remaining arguments are moot in view of new grounds of rejection.

### *Claim Objections*

4. Claims 1-5, 7, 10, and 12-17 are objected to because of the following informalities:

Claim 1 recites the limitation "clock" at line 26, it should be "block".

Claim 1 reads “whereby the validity from the invalid block is determined by a two-bit counter, which is added to each commit block (C0, C1)" in lines 28-30, it should be “whereby the validity of the invalid commit block is determined by a two-bit counter (C0, C1), which is added to each commit block".

Claims 1 and 15 recites the limitation “a bit in the commit block" in line 13. It should be “the bit existing in the commit block”.

Claim 10 ends with “;” but the claims must end with full stop (.), please make appropriate corrections.

Claim 14 recites the term MSB, however it is not clear what MSB stands for, most significant bit or most significant byte or something else.

Appropriate corrections are required.

### *Claim Rejections - 35 USC § 112*

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-5, 7 and 15-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation “replacing individual memory blocks by each other" in line 15, however it is not clear what applicant mean by “replacing blocks by each other”, two valid blocks are replaced by each other, two empty block are replaced by

each other, valid and invalid blocks are replaced by each other or old and new blocks are replaced by each other?

Claim 1 recites the limitations "the unchanged data", "the old data blocks", "the concerned logical blocks", "the field", "the block", "the invalid commit block" in lines 17, 21, 22, 23, 27 and 28. There is insufficient antecedent basis for these limitations in the claim.

Claim 3 recites the limitations "the block number" and "the number" in line 2. There is insufficient antecedent basis for these limitations in the claim.

Claim 5 recites the limitation "the leading block" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claims 1 and 15 recites the limitation "the corresponding memory block" in lines 13-14. There is insufficient antecedent basis for this limitation in the claims.

Claims 2, 4, 7 and 16-17 are also rejected due to their dependency on rejected claims.

### *Claim Rejections - 35 USC § 102*

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 10 and 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Sassa (US 6,098,077).

As per claim 10, Sassa teaches a device with a persistent memory and a block structure comprising (figs. 2 and 3):

a) a memory managing system using a block oriented memory structure (fig. 3);

b) blocks with the same, length and identifying them by their logical block number (LBN) (col. 1, lines 35-41, col. 9, lines 10-18);

c) a block allocation table (BAT) to resolve the logical block number to a physical block number (PBN) and its physical address (col. 9, lines 10-20);

d) a linkage between blocks by writing the LBN of the following block to the header of the leading one (col. 6, line 39 – col. 7, line 7).

As per claim 13, Sassa teaches a device according to claim 10 characterized in that the BAT is held in persistent memory (EEPROM) (col. 9, lines 40-41, col. 10, lines 8-10).

As per claim 14, Sassa teaches a device according to claim 10 characterized in that the BAT is held in non-persistent memory and re-initialized on startup (col. 9, lines 39-40), whereby the structure of a memory block consists of a block header and a data area and the header consists of status data containing MSB logical block number of the own block number and MSB of the next block number (fig. 4, col. 6, line 39 - col. 7, line 7, ("The “logical address” indicates a logical address of the block. The "linkage address” indicates a logical address of a block to be linked with this block”).

### *Claim Rejections - 35 USC § 103*

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sassa (US 6,098,077) as applied to claim 10 above and further in view of Gonzalez et al. (US 6,684,289).

As per claim 12, Sassa teaches all the limitations of claim 10 and further teaches blocks with fixed block size (col. 6, lines 25-30), however he fails to teach block containing several independent memory segments, belonging to different logical data units. Gonzalez teaches block containing memory segments belonging to different logical data (Gonzalez, fig. 8, col. 3, and lines 4-10). It would have been obvious to one having ordinary skill in the art at the time of the invention to use block containing memory segments belonging to different logical data as taught by Gonzalez in the system of Sassa to make efficient use of particular block and increase amount of data stored (Gonzalez, col. 3, lines 14-18, lines 26-29).

11. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sassa (US 6,098,077) and further in view of Lasser (US 6,883,114) and Spiegel et al. (US 6,571,326).

As per claim 15, Sassa teaches a method for memory management in smart card controller or similar restricted hardware environment by writing of data into a data space in a persistent memory (figs. 2, 3), the method comprising:

a) splitting the persistent memory into blocks with fixed data length having logical block numbers (LBN) (col. 1, lines 35-41, col. 9, lines 10-18);

b) selecting the size of blocks as such that it is equal to, or equivalent to an integer ratio of, the length of a page in EEPROM to the physical size of the pages of the EEPROM memory existing on the card (col. 6, lines 25-30);

c) providing a Block Allocation Table (BAT) in order to calculate the physical place of the block in memory from the logical block number (col. 6, lines 32-39, col. 9, lines 10-20);

d) defining a bit existing in each block header, whereby this bit corresponds to a bit existing in a commit block (fig. 3, data blocks n and n+1 are commit blocks, col. 8, lines 49-61).

Sassa fails to teach where toggling of a bit in the commit block toggles the validity of the corresponding memory block. Lasser teaches a use of commit bit, where by toggling of a bit in commit block toggles the validity of the corresponding memory block (Lasser, figs. 5, 6A-6E, col. 9, line 3 – col. 10, line 62; col. 9, line 3 – col. 10, line 62, the “R” setting “1” or “0” or vise versa). It would have been obvious to one having ordinary skill in the art at the time of the invention to use commit bit as taught by Lasser in the system of Sassa to provide consistent data storage (Lasser, col. 2, lines 35-51).

Spiegel also teaches toggling of valid bit toggles the validity of data block (Spiegel, col. 2, lines 20-22). It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize commit bit (valid/invalid bit) to effectively erase data using single bit as taught by Spiegel (col. 2, lines 22-23).

As per claim 16, Sassa, Lasser or Spiegel explicitly fail to teach commit bits are managed on a physical level, however it is inherent that toggling the values of the bits (e.g. from "0" to "1" or vise versa) managed at physical level.

### *Allowable Subject Matter*

12. Claim 1 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

13. Claims 2-5, 7, and 17 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

### *Conclusion*

14. The examiner also requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

15. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAUSHIKKUMAR PATEL whose telephone number is (571)272-5536. The examiner can normally be reached on 7.30 am - 4.00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hyung S Sough/
Supervisory Patent Examiner, Art Unit 2188
06/20/08

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